AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (*Currently Amended*) A delay analysis system for making a delay analysis of a logic circuit,

said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits,

wherein, for at least one of said plurality of circuits, said library further comprises logical operation information representing correspondence between ~~a~~ logical state transitions at ~~value of~~ each input terminal of said at least one circuit and ~~a~~ logical state transitions at ~~value of~~ each output terminal of said at least one circuit, and said delay information for said at least one circuit is based upon a logical state transition at an input terminal and its corresponding logical state transition at an output terminal ~~input terminal signal transition type and a logical state~~ as represented by said logical operation information for said at least one circuit, and

when making a delay analysis of the logic circuit comprising said at least one circuit, a delay time is selected from said delay time information according to the type of logical state transitions present at selected input and output terminals ~~input terminal signal transition type and current logical state~~ of said at least one circuit.

2. (*Currently Amended*) A delay analysis system for making a delay analysis of a logic circuit, said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits,

wherein, for at least one of said plurality of circuits, said library further comprises logical operation information representing correspondence between ~~a~~ logical state transitions at ~~value of~~ each input terminal of said at least one circuit and ~~a~~ logical state transitions at ~~value of~~ each output terminal of said at least one circuit, and said delay information for said at least one circuit is based upon a logical state transition at an input terminal and its corresponding logical state transition at an output terminal ~~input terminal signal transition type and a logical state~~ as represented by said logical operation information for said at least one circuit, and

when making a delay analysis of a logic circuit, a delay time between a selected ~~an~~ input terminal and a selected ~~an~~ output terminal of said at least one circuit is selected from said delay time information according to the type of logical state transitions present at said selected input and output terminals ~~input terminal signal transition type and current logical state~~ of said at least one circuit.

3. (*Currently Amended*) A method for making a delay analysis of a logic circuit, comprising the steps of:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information representing correspondence between ~~a~~ logical state transitions at ~~value of~~ each input terminal and ~~a~~ logical state transitions at ~~value of~~ each output terminal of at least one of said plurality of circuits, said delay information for said at least one circuit is based upon a logical state transition at an input terminal and its corresponding logical state transition at an output terminal ~~input terminal signal transition type and a logical state~~ as represented by said logical operation information for said at least one circuit; and

if the logic circuit comprises said at least one circuit, selecting the delay time of said at least one circuit from said delay time information according to the type of logical state transitions present at selected input and output terminals ~~input terminal signal transition type and current logical state~~ of said at least one circuit.

4. (*Currently Amended*) A computer-readable medium having stored thereon a program for executing:

~~(a)~~ a process step comprising:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information representing correspondence between ~~a~~ logical state transitions at ~~value of~~ each input terminal and ~~a~~ logical state transitions at ~~value of~~ each output terminal of each one of said plurality of circuits, said delay information for said at least one circuit is based upon a logical state transition at an input terminal and its corresponding logical state transition at an output terminal ~~input terminal signal transition type and a logical state~~ as represented by said logical operation information for said at least one circuit; and

if a logic circuit comprises said at least one circuit, selecting the delay time of said at least one circuit from said delay time information according to the type of logical state transitions present at selected input and output terminals ~~input terminal signal transition type and current logical state~~ of said at least one circuit; and

~~(b)~~ a process step of performing a delay calculation using said selected delay time as a propagation delay time of said at least one circuit.